PCI-SIG ENGINEERING CHANGE REQUEST

TITLE:	Manufacturing Mode
DATE:	October 30~~24~~, 2018
AFFECTED DOCUMENT:	PCI Express SFF-8639 Module Specification Rev 3.0 Ver 1.0
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Part I

1. Summary of the Functional Changes

High Volume Manufacturing (HVM) benefits from the ability to set manufacturing specific SFF-8639 Module modes that enable multiplexing of standard connector pins for manufacturing test specific use. This ECR is to define a method to allow the Host to enable Manufacturing Mode on the SFF-8639 Module through the standard interface connector.

The Manufacturing Mode solution proposed is consistent with that already approved in SNIA SFF-TA-1001 Revision 1.1 for SFF-8639 use.

2. Benefits as a Result of the Changes

Support for a Manufacturing Mode state, set using standard interface signals, allows manufacturing modes and signal multiplexing to support test signaling without requiring a separate connector. Separate connectors add cost not just as SFF-8639 Module connector costs, but also for non-interface connector insertion handling. Manual cabling is unreliable, and prevents effective use of automation (i.e. robotoic insertion/removal).

Setting Manufacturing Mode state and the associated pin signal multiplexing through the standard connector allows greatly reduced HVM system costs through reduced insertion counts and automation support.

The Manufacturing Mode solution proposed is consistent with that already approved in SNIA SFF-TA-1001 Revision 1.1 for SFF-8639 use.

3. Assessment of the Impact

The Manufacturing Mode pin states are an optional feature, only implemented if SFF-8639 Module manufacturers require it. Uses pins already ratified for the same use in SNIA SFF-TA-1001 Revision 1.1 for SFF-8639 use.

4. Analysis of the Hardware Implications

Adds two optional pins previously defined as “Reserved”, S15 and E16, and shares the DualPortEn# signal on pin E25. These are optional signals, so only add cost if SFF-8639 Module manufacturers require these pins to be populated on the SFF-8639 connector.

If this optional feature is supported, then Manufacturing Test systems and SFF-8639 Modules are responsible to designing the pin signal multiplexing required specific to SFF-8639 Module manufacturer needs.

5. Analysis of the Software Implications

Optional support for HVM Tester System software only. If this feature is implemented, it is disabled when the SFF-8639 Module is configured for customer shipment.

SFF-8639 Module customer firmware will not support Manufacturing Mode, so no impact other than insuring all pin multiplex circuits are securely set to standard customer use states.

6. Analysis of the C&I Test Implications

No C&I Tests of the optional Manufacturing Mode signaling are envisioned for PCI-SIG.

7. Analysis of the Virtualization Implications

No impact. SR-IOV is not affected.

Part II

Detailed Description of the change

"Change Section 1.3, Terms and Definitions, page 9 as follows:"

HPTn	Host Port Type operational mode configuration setting signals

"Change Section 1.4, Reference Documents, page 10 as follows:"

- *SFF-TA-1001*, Revision 1.1

"Change Section 1.7, Electrical Overview, page 12 as follows:"

- DualPortEn#: This signal is asserted to enable Dual port mode of the SFF-8639 Module and de-assert to default to a single x4 port, optional. This signal is also used in conjunction with HPT0 and HPT1 to set optional Host Port Type.
- HPT0 and HPT1: These signals are asserted, in~~used in~~ conjunction with DualPortEn#, to set the Host Port Type~~which Host System sets to enable~~ of the SFF-8639 Module, optional ~~Host Port Type state~~.

The signals HPT0, HPT1, REFCLK+, REFCLK-, REFCLKB+, REFCLKB-, SMBCLK, SMBDAT, PERST#, PERSTB#, ACTIVITY#, DualPortEn#, CLKREQ#, PWRDIS, and WAKE# are described in Chapter 2, *Auxiliary Signals*.

"Change Section 2.0, Auxiliary Signals, page 15 as follows:"

- DualPortEn# (optional): This signal is an open drain pulled high by the SFF-8639 Module and asserted low by the system to enable Dual port mode of the SFF-8639 Module. This signal is also used in conjunction with HPT0/HPT1 to set optional Host Port Type.
- HPT0/HPT1 (optional): These signals are open drain pulled high by the SFF-8639 Module and asserted low by the system to enable Host Port Type.

"Change Section 2.5, DualPortEn#, page 30 as follows:"

2.5. DualPortEn# (Optional)

When de-asserted, the SFF-8639 Module is configured as a single x4 PCI-Express device. When asserted, the SFF-8639 Module is configured as two independent x2 PCI-Express devices. As independent ports, the absence of the A-side port (or B-side port) on the system or module must not alter the operation of the other port.

Support of DualPortEn# is optional. The system asserts the open-drain signal by driving it low. Electrical characteristics are described in Table 2-4. Control signal mapping is detailed in Table 2-3. DualPortEn# is valid only when supported by both the system and module.

Table 2-3. DualPortEn# Control Signal Map

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2.5.1. DualPortEn# use for Host Port Type Control

DualPortEn# is also used in conjunction with HPT0/HPT1 to set Host Port Type states. See section 2.9 for details.

"Add New Section 2.9, HPT0/HPT1, page 32 as follows:"

2.9. HPT0/HPT1 (Optional)

Support for signals HPT0, HPT1 is optional. The system asserts these open-drain signals by driving them low. Electrical characteristics are described in Table 2-5. Control signal mapping is detailed in Table 2-4.

These signals are valid only when supported by both the system and module.

Table 2-4. Host Port Type Signal States

HPT0 Pin S15	HPT1 Pin E16	DualPortEn# Pin E25	Host Port Mode
Open	Open	Open	Host Port Quad PCIe Single x4
Open	Open	Gnd	Host Port Quad PCIe Dual x2
Gnd	Gnd	Gnd	Manufacturing Mode

Note: All other signal states are outside scope of this specification (See SFF-TA-1001).

2.9.1. Manufacturing Mode

Manufacturing Mode may be enabled by the device when the HPT0, HPT1, and DualPortEn# signals are set as specified in Table 2-4. Manufacturing Mode is vendor specific and must only be used during device manufacturing.

Post device manufacturing, a mechanism must be deployed to prevent unauthorized access to the manufacturing mode. This mechanism is vendor specific, outside the scope of this specification.

"Change Section 2.9 to 2.10, Auxiliary Signal Parametric Specifications, page 33 as follows:"

2.10. Auxiliary Signal Parametric Specifications

2.10.1. DC Specifications

The DC specifications for ACTIVITY#, DualPortEn#, PERST#, WAKE#, CLKREQ#, PERSTB#, IfDet#, PRSNT#, SMBus, HPT0, HPT1 are given in Table 2-5.

Table 2-5. Auxiliary Signal DC Specifications - ACTIVITY#, DualPortEn#, PERST#, WAKE#, CLKREQ#, PERSTB#, IfDet#, PRSNT#, ~~and~~ SMBus, HPT0, and HPT1

"Change Section 5.1, Connector Pinout, Table 5-1 as follows:"

Table 5-1. SFF-8639 PCI Express Connector Pinout

Pin	Mate	Name	Type	Description
P1	3rd	WAKE#	Bi-Dir	Signal for Link reactivation
P2	3rd	-	-	Outside scope of this specification (See SFF-8639)
P3	2nd	PWRDIS	Output	Power disable
P4	1st	IfDet#	Input	Interface Type Detect
P5	2nd	Ground	Ground	Ground
P6	2nd	Ground	Ground	Ground
P7	2nd	-	-	Outside scope of this specification (See SFF-8639)
P8	3rd	-	-	Outside scope of this specification (See SFF-8639)
P9	3rd	-	-	Outside scope of this specification (See SFF-8639)
P10	2nd	PRSNT#	Input	Presence detect
P11	3rd	ACTIVITY#	Input	Activity indicator
P12	1st	Ground	Ground	Ground
P13	2nd	+12 V Precharge	Power	+12 V Precharge power for SFF-8639 Module
P14	3rd	+12 V	Power	+12 V power for SFF-8639 Module
P15	3rd	+12 V	Power	+12 V power for SFF-8639 Module
S1	2nd	Ground	Ground	Ground

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Pin	Mate	Name	Type	Description
S2	3rd	-	-	Outside scope of this specification (See SFF8639)
S3	3rd	-	-	Outside scope of this specification (See SFF8639)
S4	2nd	Ground	Ground	Ground
S5	3rd	-	-	Outside scope of this specification (See SFF8639)
S6	3rd	-	-	Outside scope of this specification (See SFF8639)
S7	2nd	Ground	Ground	Ground
S8	2nd	Ground	Ground	Ground
S9	3rd	-	-	Outside scope of this specification (See SFF8639)
S10	3rd	-	-	Outside scope of this specification (See SFF8639)
S11	2nd	Ground	Ground	Ground
S12	3rd	-	-	Outside scope of this specification (See SFF8639)
S13	3rd	-	-	Outside scope of this specification (See SFF8639)
S14	2nd	Ground	Ground	Ground
S15	3rd	HPT0	Output	Host Port Type-0
S16	2nd	Ground	Ground	Ground
S17	3rd	PETp1	Diff-Pair	Transmitter differential pair, Lane 1
S18	3rd	PETn1	Diff-Pair	Transmitter differential pair, Lane 1
S19	2nd	Ground	Ground	Ground
S20	3rd	PERn1	Diff-Pair	Receiver differential pair, Lane 1
S21	3rd	PERp1	Diff-Pair	Receiver differential pair, Lane 1
S22	2nd	Ground	Ground	Ground
S23	3rd	PETp2	Diff-Pair	Transmitter differential pair, Lane 2
S24	3rd	PETn2	Diff-Pair	Transmitter differential pair, Lane 2
S25	2nd	Ground	Ground	Ground

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Pin	Mate	Name	Type	Description
S26	3rd	PERn2	Diff-Pair	Receiver differential pair, Lane 2
S27	3rd	PERp2	Diff-Pair	Receiver differential pair, Lane 2
S28	2nd	Ground	Ground	Ground
E1	3rd	REFCLKB+	Diff-Pair	Reference clock for second x2 port
E2	3rd	REFCLKB-	Diff-Pair	Reference clock for second x2 port
E3	3rd	+3.3 Vaux	Power	+3.3 V auxiliary power
E4	3rd	CLKREQ#/PERSTB#	Bi-Dir	Clock request/Fundamental reset for second x2 port
E5	3rd	PERST#	Output	Fundamental reset (if Dual port mode enabled, first x2 port)
E6	3rd	-	-	Outside scope of this specification (See SFF-TA-1001)
E7	3rd	REFCLK+	Diff-Pair	Reference clock (if Dual port mode enabled, first x2 port)
E8	3rd	REFCLK-	Diff-Pair	Reference clock (if Dual port mode enabled, first x2 port)
E9	2nd	Ground	Ground	Ground
E10	3rd	PETp0	Diff-Pair	Transmitter differential pair, Lane 0
E11	3rd	PETn0	Diff-Pair	Transmitter differential pair, Lane 0
E12	2nd	Ground	Ground	Ground
E13	3rd	PERn0	Diff-Pair	Receiver differential pair, Lane 0
E14	3rd	PERp0	Diff-Pair	Receiver differential pair, Lane 0
E15	2nd	Ground	Ground	Ground
E16	3rd	HPT1	Output	Host Port Type-1
E17	3rd	PETp3	Diff-Pair	Transmitter differential pair, Lane 3
E18	3rd	PETn3	Diff-Pair	Transmitter differential pair, Lane 3
E19	2nd	Ground	Ground	Ground

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Pin	Mate	Name	Type	Description
E20	3rd	PERn3	Diff-Pair	Receiver differential pair, Lane 3
E21	3rd	PERp3	Diff-Pair	Receiver differential pair, Lane 3
E22	2nd	Ground	Ground	Ground
E23	3rd	SMBCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	3rd	SMBDAT	Bi-Dir	SMBus (System Management Bus) data
E25	3rd	DualPortEn#	Output	Dual port Enable, and Host Port Type control